WHAT IS CLAIMED IS:

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1. A method for transferring packets between a plurality of nodes including a first node, a second node, and a third node connected to one another by a bus, the method comprising the steps of:

(a) transferring a write packet from the first node to the second node;

(b) storing data addressed to the third node in the write packet at the second node; and

(c) transferring the write packet from the second node to the third node.

2. The packet transfer method according to claim 1, wherein the write packet includes a data portion for storing data, and wherein the data portion is blank.

3. The packet transfer method according to claim 1, wherein the first node has information indicating that a plurality of the second nodes substantially simultaneously transfer packets to a plurality of the third nodes, and wherein the write packet transfer step (a) includes transferring the write packet to the plurality of the second nodes based on the information.

4. The packet transfer method according to claim 1, wherein the write packet includes a header portion and a data portion, and wherein the data portion stores identification information indicating whether the data portion is blank.

5. The packet transfer method according to claim 1, wherein the write packet transfer step (a) includes transferring a guide packet to the second node storing guide

information indicating the state of the write packet, before the first node transfers the write packet, and wherein the data storing step (b) includes writing the guide information to the guide packet to indicate that data has been written to the write packet.

6. The packet transfer method according to claim 1, further comprising the steps of:

(d) transferring a data packet from the first node to the second node;

(e) processing the data stored in the data packet at the second node; and

(f) transferring the data packet including the processed data to the third node, wherein the write packet transfer step (a) is performed after the data packet transfer step (d).

7. The packet transfer method according to claim 1, wherein the write packet transfer step includes transferring the write packet from the first node to the second node at predetermined time periods.

8. The packet transfer method according to claim 1, further comprising the step of padding the data stored in the write packet so that the amount of the data is substantially the same as the data storage capacity of the write packet.

9. A method for transferring packets between a plurality of connected nodes including a first node, a second node, and a third node, the method comprising the steps of:

transferring a first packet storing first data from the first node to the second node;

processing the first data stored in the first packet

and temporarily storing the processed first data at the second node;

transferring a second packet storing second data from the first node to the second node;

rewriting the second data stored in the second packet to the processed and temporarily stored first data at the second node; and

transferring the second packet storing the processed first data to the third node.

10. A packet transfer control circuit incorporated in a first node to transfer a packet to a second node, connected to the first node, wherein the packet includes a data portion for storing data, the control circuit comprising:

an identification circuit for identifying whether the data portion is blank; and

a processor connected to the identification circuit for writing data to the data portion when the data portion of the packet is blank.

11. The packet transfer control circuit according to claim 10, wherein the processor pads the data stored in the packet until the amount of the data is substantially the same as the data storage capacity of the data portion.

12. A packet transfer control circuit incorporated in a first node to transfer a packet to a second node and a third node, which are connected to the first node, wherein the packet includes a data portion for storing data, and wherein the second node is downstream from the first node and the third node is upstream from the first node, the control circuit comprising:

a processor for retaining data addressed to the third node and rewriting the data stored in the data portion of

the packet received by the first node from the second node when the stored data is addressed to the third node.

13. A packet transfer control circuit incorporated in a first node to transfer a plurality of packets to a second node and a third node, which are connected to the first node, wherein each of the packets includes a data portion for storing data, the control circuit comprising:

a processor for transferring a write packet, the data portion of which is blank, to the second and third nodes so that the second and third nodes substantially simultaneously store data in the data portion of the write packet.

14. The control circuit according to claim 13, wherein the write packet further includes an identifier for storing information indicating whether the data portion is blank.

15. The control circuit according to claim 13, wherein the processor transfers a guide packet storing guide information indicating a state of the write packet before transferring the write packet from the first node, and wherein the guide information written to the guide packet indicates that data has been written to the write packet when the second node stores data.

16. A packet transfer control circuit incorporated in a first node to transfer packets to a plurality of second nodes, which are connected to the first node, wherein each of the packets includes a data portion for storing data, the control circuit comprising:

a processor for transferring to the second nodes a write packet, the data portion of which stores data, and then a further write packet, the data portion of which is blank, wherein each of the second nodes stores data in the

blank data portion.

17. The control circuit according to claim 16, wherein the write packet further includes an identifier for storing information indicating whether the data portion is blank.

18. The control circuit according to claim 16, wherein the processor transfers a guide packet storing guide information indicating the state of the write packet before transferring the write packet from the first node, and wherein the guide information written to the guide packet indicates whether data has been written to the write packet when each of the second nodes stores data.

19. A packet transfer control circuit of a first network node, comprising:

an input interface circuit for receiving a packet from a second network node connected to the first network node, the received packet being one of a normal packet type and a write packet type, and the received packet comprising at least a header portion and a data portion;

an input link layer processing circuit, connected to the input interface circuit, for receiving the received packet therefrom, reading the header portion of the packet to determine the packet type, and if the received packet is a normal packet, also determining an addressee of the packet;

an identification circuit, connected to the input link layer processing circuit, for receiving a write packet type of packet from the input link layer processing circuit, checking an identifier of the data portion of the write packet to determine whether the data portion of the write packet is blank and to determine an addressee of the write packet, wherein the identification circuit generates a

control signal if the data portion is blank;

a processor, connected to the identification circuit and the input link layer processing circuit, wherein the input link layer processing circuit passes the received packet directly to the processor if the received packet is addressed to the first node and is a normal type packet, wherein the processor receives the packet data from the identification circuit if the packet is a write type packet, and wherein the processor receives the control signal from the identification circuit and pads the data portion of the packet in order to fill the data portion of the packet when the control signal indicates that the data portion is blank;

a memory, connected to the processor, for storing the packet data processed by the processor;

an output link layer processing circuit, connected to the processor and to the input link layer processing circuit, for receiving the packet therefrom and preparing a transmission packet from the packet, wherein the input link layer processing circuit passes a normal type packet not addressed to the first node directly to the output link layer processing circuit; and

an output interface circuit, connected to the output link layer processing circuit, for receiving the transmission packet therefrom and transmitting the transmission packet over a bus to another node.

20. The packet transfer control circuit of claim 19, wherein the packets are transferred between nodes over an IEEE 1394 compatible bus.

21. The packet transfer control circuit of claim 19, further comprising:

an input physical layer processing circuit, connected between the input link layer processing circuit and the

input interface circuit, for receiving the packets from the input interface circuit and transferring them to the input link layer processing circuit.

22. The packet transfer control circuit of claim 21, further comprising:

an output physical layer processing circuit connected between the output link layer processing circuit and the output interface circuit, for transferring the transmission packet from the output link layer processing circuit to the output interface circuit.

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